REMARKS

The Office Action of January 12, 2006 has been received and its contents carefully considered.

The present Amendment cancels claims 13 and 14. The present Amendment also revises the remaining claims where propriate to correct informalities and to improve form of the claims under the US claim-drafting practice. In view of these revisions, it is respectfully submitted that the claim objection set forth on pages 2-3 of the Office Action have been overcome.

On pages 3-19, the Office Action rejects all of the claims for obviousness based on US patent 6,242,269 to Whetsel in view of US patent 6,169,500 to Ericsson et al. This latter reference will hereafter be called simply "Ericsson" for the sake of convenience. For the reasons discussed below, it is respectfully submitted that the claims are patentable over these references.

Claim 1 recites "m scan chains... each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series." At the top of page 4, the Office Action draws attention to element 924 in Figure 8 of the Whetsel reference. However, the Whetsel reference just calls element 924 a "scan path," and does not say that it includes logic circuits alternating with scan registers. To Whetsel, a "scan path" appears to be just a serial path through functional circuitry (see column 2 of the reference, lines 53-56).

Claim 1 also recites that each of the scan chains includes "a first logic circuit having a data input terminal, a first scan register connected to the first logic circuit, the first scan register having a test input register and a last scan register having an output terminal." At the top of page 4, the Office Action asserts that elements 800 and 844 in Whetsel's Figure 8 meet these limitations. However, Whetsel's elements 800 and 844 are not part of his scan path 924 and, moreover, are not disclosed as including a first logic circuit and a last scan register.

Claim 1 also provides that the scan registers are operated in response to a clock signal, and that a serial/parallel conversion circuit and a parallel/serial conversion circuit are responsive to a multiplied clock signal. The Office Action acknowledges that Whestel does not disclose this, but draws attention to the Ericsson reference. The Ericsson reference discloses a serial/parallel and parallel/serial converter. However, an ordinarily skilled person would have had no reason to think that different clock frequencies would be useful in Whetsel's device simply because they are useful in parallel/serial conversion. Just what is it about Ericsson's converter that would make an ordinarily skilled person think that it would be useful to operate Whetsel's scan paths at one frequency and his scan distributors and collectors at a different frequency?

Turning now to independent claim 7, this claim recites "a plurality of scan chains each of which includes a first logic circuit having a data input terminal, a first scan register connected to the first logic circuit, the first register having a test input terminal and a last scan register having an output terminal." On page 10, the Office Action characterizes Whetsel's element 800 as a first scan register connected to a first logic

circuit and appears to characterize Whetsel's element 900 as a test input terminal of a first scan register. However, Ericsson's element 900 is not part of his element 800.

Claim 7 also provides that scan registers are operated in response to a clock signal and that conversion circuits respond to a multiplied clock signal. For the reasons noted above with respect to claim 1, it is respectfully submitted that Ericsson would not have motivated an ordinarily skilled person to modify Whetsel so to achieve this feature.

On pages 19-22, the Office Action rejects independent claims 1, 7, and 13 (now cancelled) for anticipation by Ericsson alone. This ground of rejection is also respectfully traversed.

As is noted previously, claim 1 provides that each of a plurality of scan chains includes a plurality of logic circuit and a plurality of scan registers that are connected alternately in series. On page 19, the Office Action draws attention to elements 71a-f in Ericsson's Figure 6. But Ericsson's Figure 6 does not show "scan chains," as the term would be understood by an ordinarily skilled person who had read the present application. Even apart from this difference, Ericsson's Figure 6 does not show a plurality of logic circuits and a plurality of scan registers that are collected alternately in series.

In the middle of page 21, the Office Action acknowledges that the Ericsson reference "does not teach the exact location of the parallel/serial converter, as disclosed in the specification." Assuming that this acknowledgement refers to claim 1 (rather than the specification of the present application), the acknowledgement itself would be enough to avoid anticipation. However, the Office Action refers to an ancient decision for the

proposition that "rearranging parts of an invention involves only routine skill in the art." The decision cited in the Office Action has clearly been superseded by Graham v. John Deere, which sets forth the analysis that is needed for references that are to be modified.

Independent claim 7 provides that each of plurality of scan chains includes "a first logic circuit having a data input terminal, a first scan register connected to the first logic circuit, the first scan register having a test input terminal, and a last scan register having an output terminal." The paragraph bridging pages 20 and 21 of the Office Action asserts that Ericsson has a plurality of scan chains, "each of which includes a first logic circuit having a data input terminal (Figure 3 "D_{in}"), a first scan register connected to the first logic circuit (Figure 3 #54), the first scan register having a test input terminal (Figure 3 #10) ...". However, if Ericsson's element 54 is to be characterized as "a first scan register" that is connected to a first logic circuit, the element 54 clearly does not have a test input terminal that is provided by Ericsson's element 10. Moreover, it is respectfully submitted that an ordinarily skilled person would not find any "scan chains" at all in the Ericsson reference.

On pages 23-26, the Office Action rejects independent claims 1, 7, and 13 (now cancelled) for obviousness based on a published US application by Kobayashi.

The Office Action takes the position that elements 120-123 in Kobayashi's Figure 1 represent a plurality of logic circuit and a plurality of scan registers connected alternately in series, in accordance with claim 1. However, Kobayashi's Figure 2 shows the internal circuitry of Kobayashi's elements 120-123, and it will be apparent that the

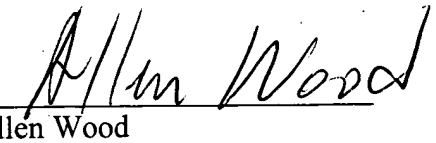
result is not a plurality of logic circuits and a plurality of scan registers connected alternately in series in accordance with claim 1.

The Office Action also draws attention to the conversion circuits 10 and 11 in Kobayashi's Figure 1. However, Kobayashi's element 10 provides parallel to serial conversion (see paragraph [0035]). It is respectfully submitted that Kobayashi's serial/parallel and parallel/serial conversion circuits are located opposite to what is recited in independent claims 1 and 7.

The remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention. They are therefore patentable along with the independent claims and need not to be further discussed.

For the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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